

ASCET-DEVELOPER 7.9

New and Noteworthy

Improve self on boarding and knowledge

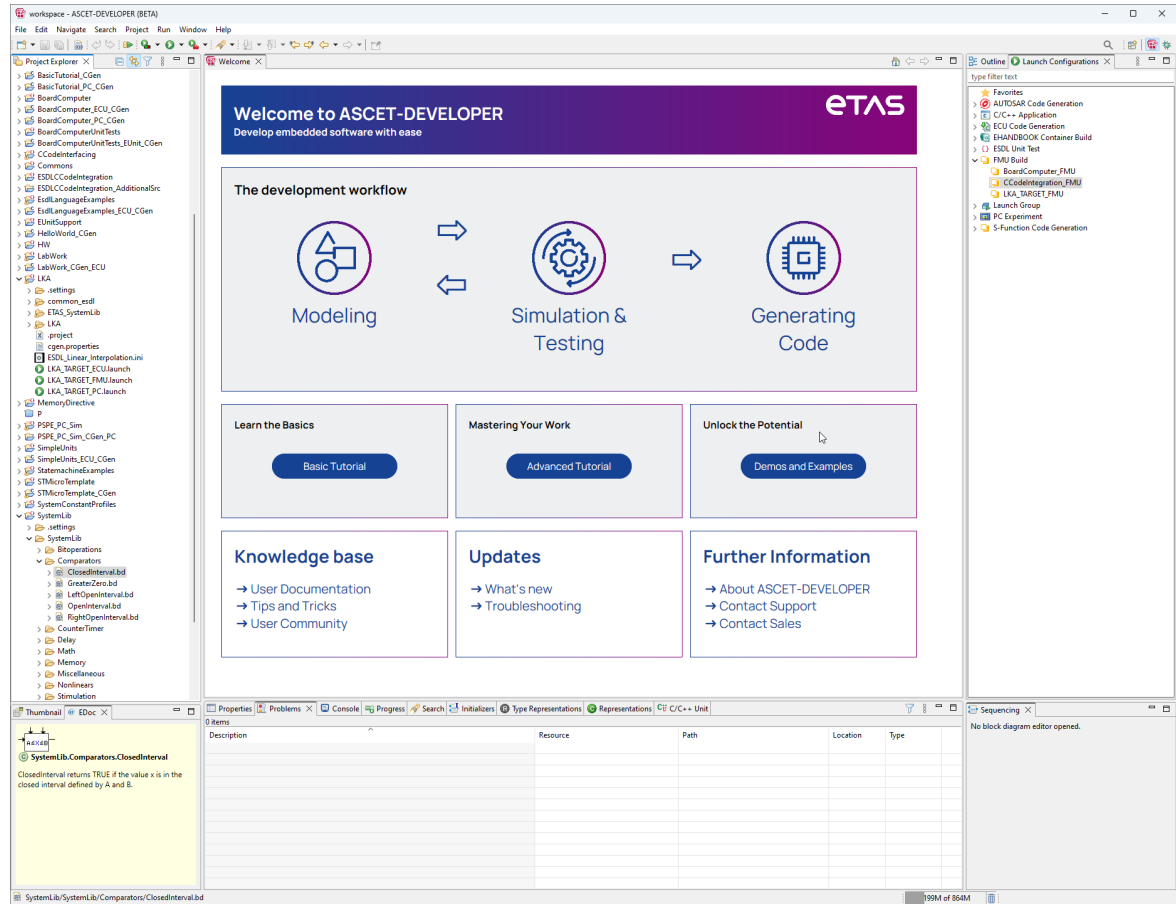
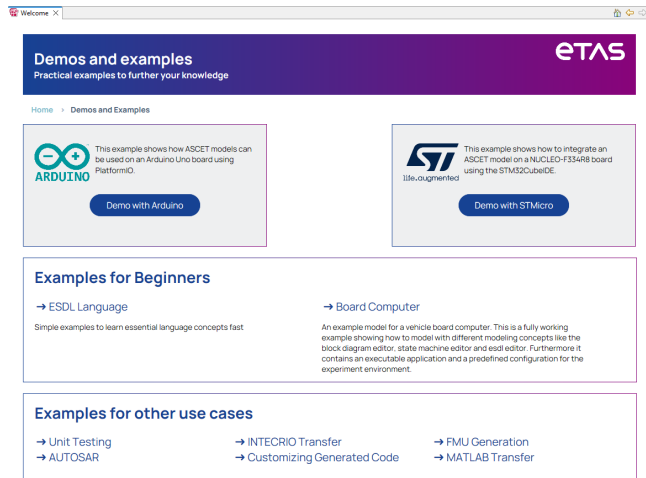
New Welcome Page and Tutorials

Pain Point

- ⊖ No easy way to self learn w/o help from ETAS Support
- ⊖ Are there good reference examples for my use cases
- ⊖ Where do I get help, ask questions

Benefit

- ⊕ User friendly and good User Experience



Improve self on boarding and knowledge

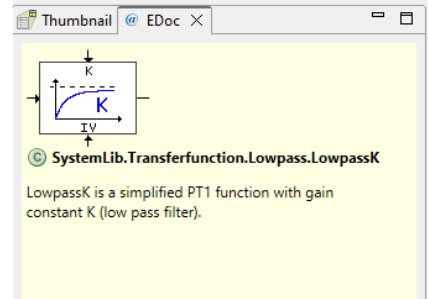
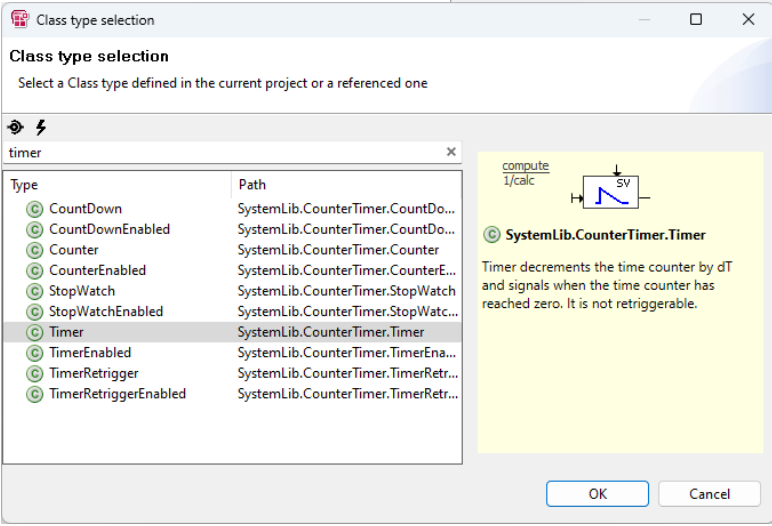
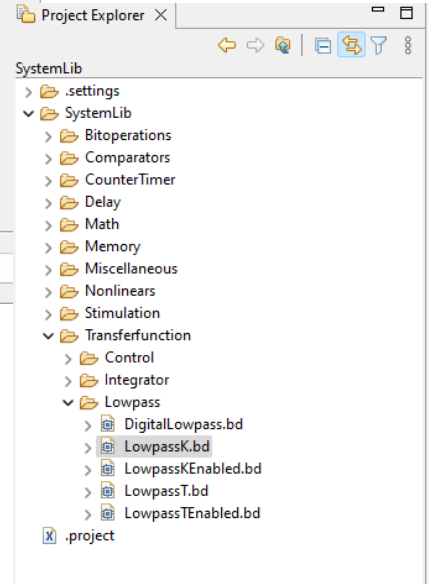
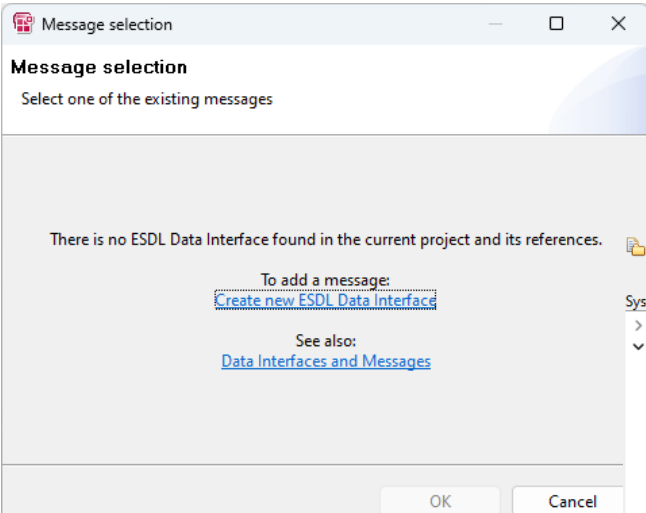
Improved Wizard Help and new Edoc view

Pain Point

- ☹ When I click on BD Editor palette button, it is empty, I don't understand what is tool expecting
- ☹ If I want to understand the type description, I need to open the definition and read the comment manually.

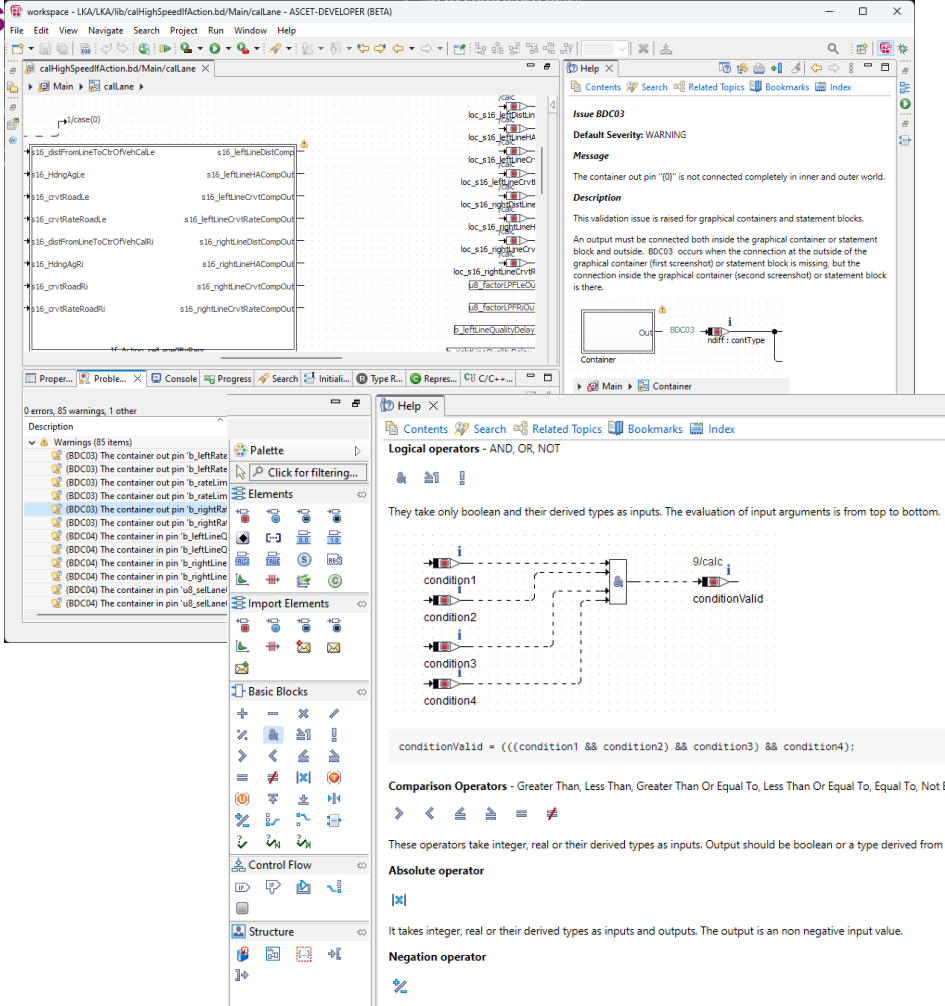
Benefit

- 😊 User friendly and good User Experience



Improve context sensitive help

Problems View , Editor and other views

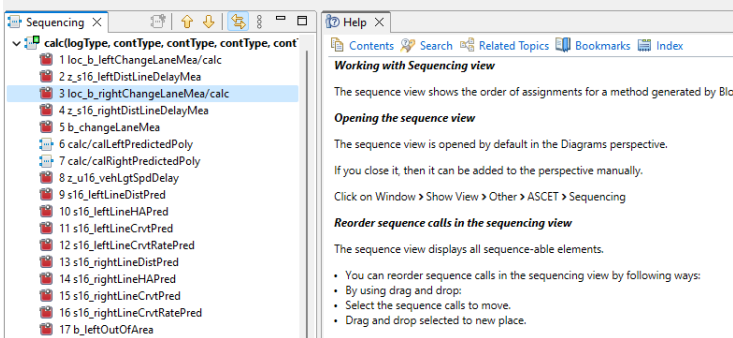


Pain Point

- ☹ Validation text is not easy to understand
- ☹ How does this view work?
- ☹ What is this palette button for?
- ☹ Time consuming to find description in user manual

Benefit

- ☺ Get help faster
- ☺ Select the issue or something in palette and press F1



Automatically create test harness

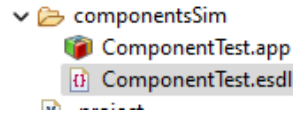
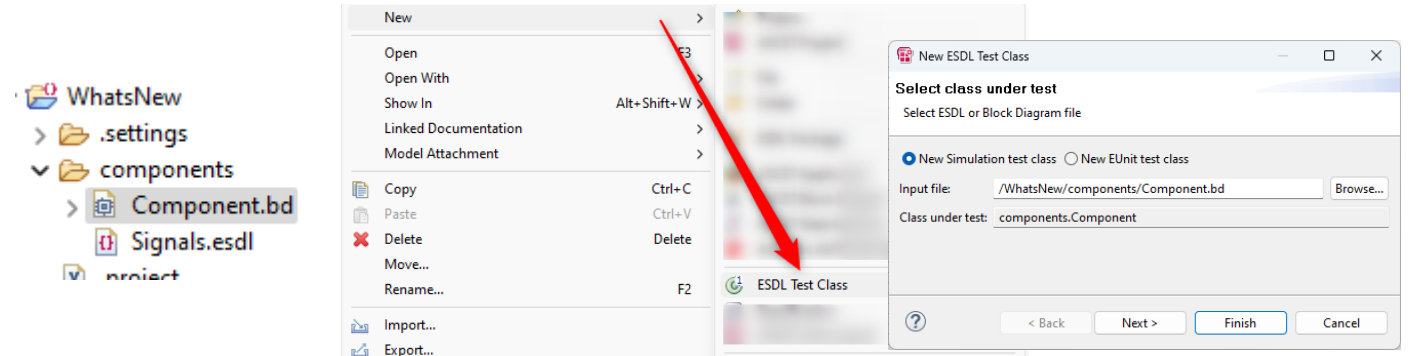
PC Simulation and Unit Testing

Pain Point

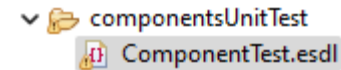
- ☹ Too many manual steps to test a class
- ☹ PC Simulation
 - ☹ Create wrapper Class
 - ☹ Create app and scheduling
 - ☹ Create stimuli
- ☹ Unit Test
 - ☹ Create Test Class
 - ☹ Manually create test methods

Benefit

- ☺ All test artefacts created quickly
- ☺ Start your test immediate and save time for boring work



```
ComponentTest.esdl ×
1 package componentsSim;
2
3 import components.Signals;
4
5 singleton class ComponentTest
6 writes Signals.message1 {
7
8   characteristic real simulate_components_Signals_message1 = 0.0;
9
10  @thread
11  public void writeToMessages() {
12    Signals.message1 = simulate_components_Signals_message1;
13  }
14 }
15 ..
```



```
ComponentTest.esdl ×
1 package componentsUnitTest;
2
3 import components.Component;
4 import components.Signals;
5 import assert.Assert;
6
7 singleton class ComponentTest
8 reads Signals.message2
9 writes Signals.message1 {
10
11   Component testee;
12   Assert Assert;
13
14   @Before
15   public void init() {
16     Signals.message1 = 0.0;
17   }
18
19   @Test
20   public void testProc_10ms() {
21     testee.proc_10ms();
22
23     // TODO: Replace this call with appropriate assertions to implement your test
24     Assert.unimplemented();
25   }
26 }
27 ..
```

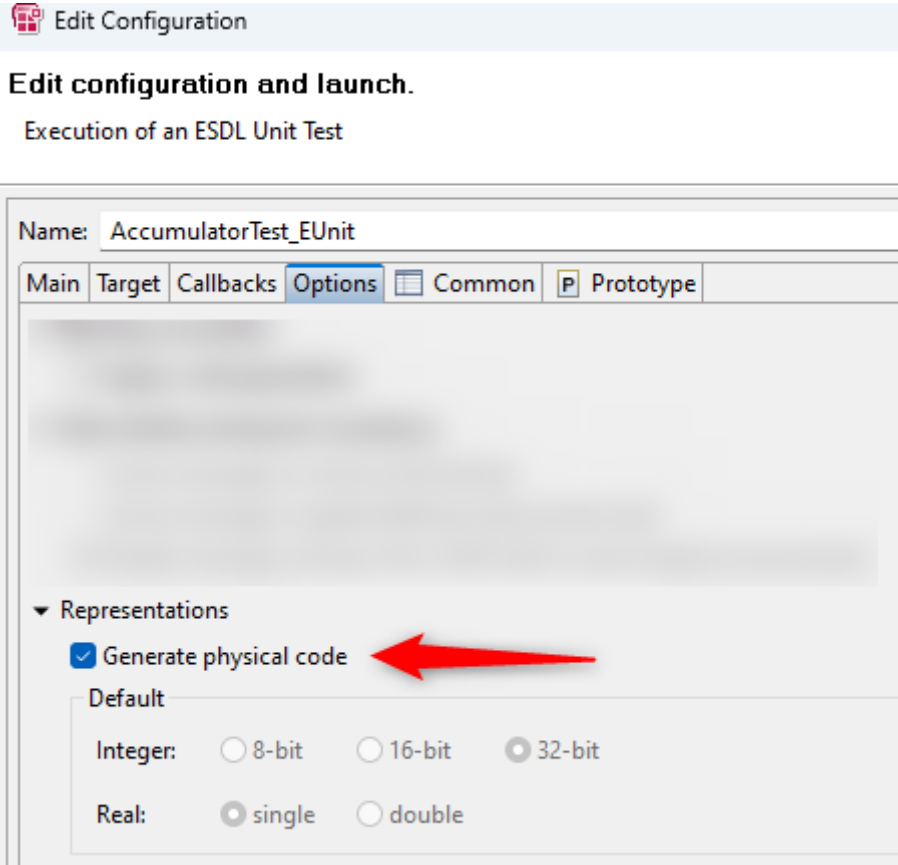
Physical code generation

Pain Point

- ☹ Unable to unit test logic independent of target representation
- ☹ With failing unit test not clear if logic or representation was reason

Benefit

- ☺ Bringing MiL/SiL like use case also to unit testing
- ☺ Run back-to-back test for every change



Group as statement block

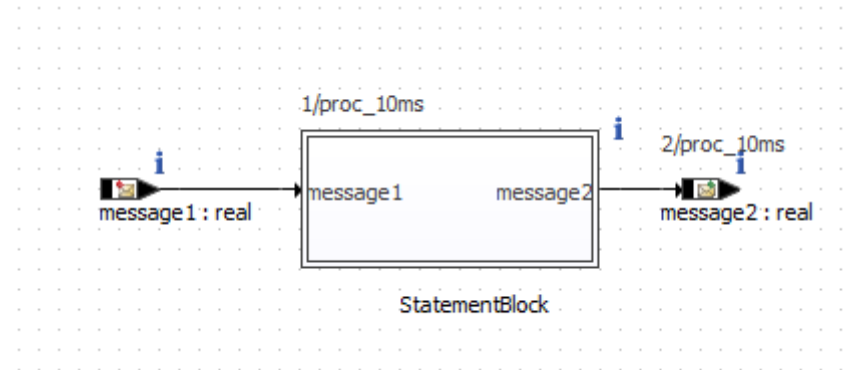
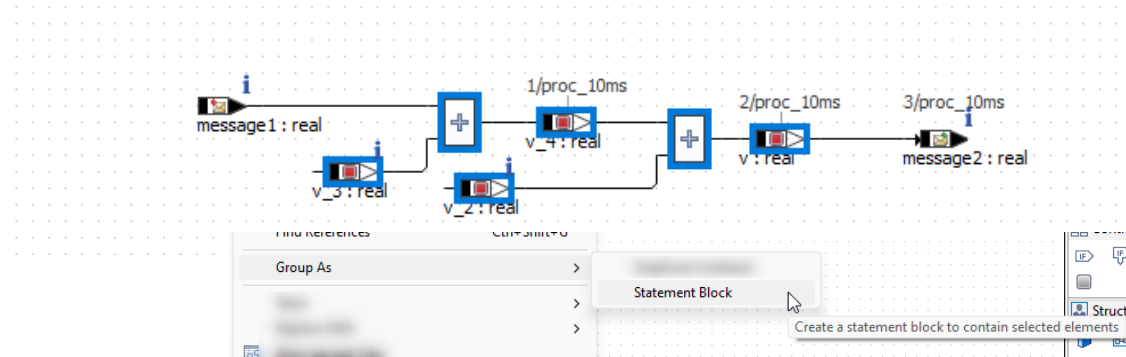
Improve refactoring

Pain Point

- ☹️ Quickly refactoring part of diagram as statement block not possible

Benefit

- 😊 Refactor complex diagrams and manage control and data flow using statement block



Integrate external code

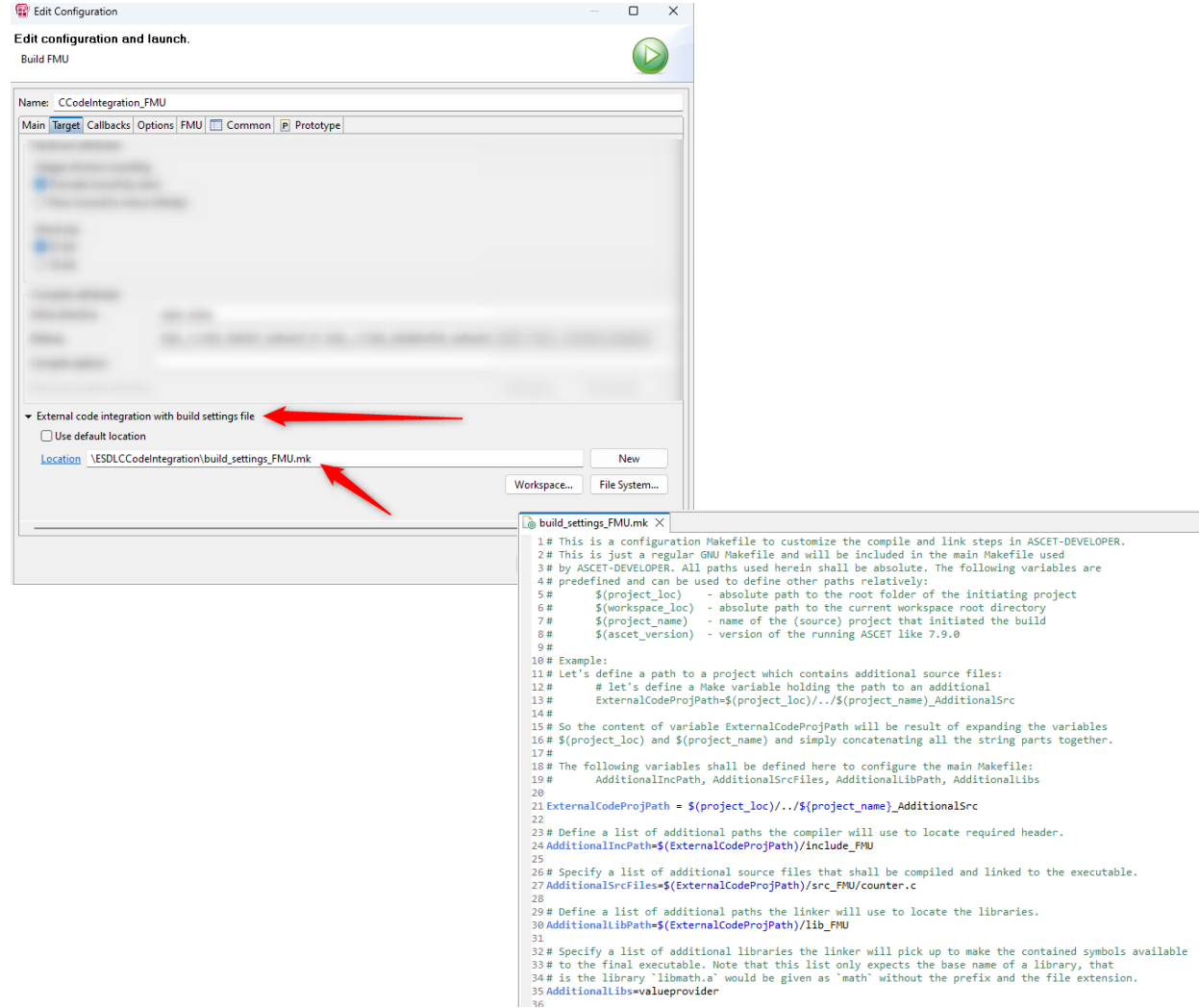
PC, EUnit, FMU Build

Pain Point

- ☹ Unable to include external code used by ASCET Model for the build

Benefit

- ☺ Easy integration and behavior dependent on external code can also be verified



Sequence number commenting

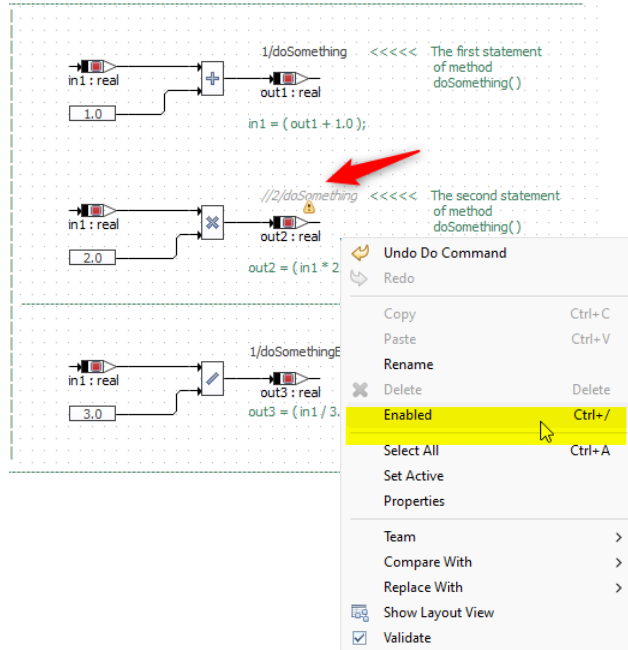
Disable code

Pain Point

- ☹ No possibility in block diagram editor to disable a sequence number execution
- ☹ In textual modeling I can comment out lines-of-code and later bring it back

Benefit

- 😊 Easy way to disable sequence number and thereby its execution
- 😊 As natural as commenting out lines of code
- 😊 No need to delete BD parts as workaround



Improved properties view in state machine editor

Faster operations

Pain Point

- ☹ To edit state machine class element properties always switch to ESDL editor

Benefit

- ☺ Stay in context and faster operations

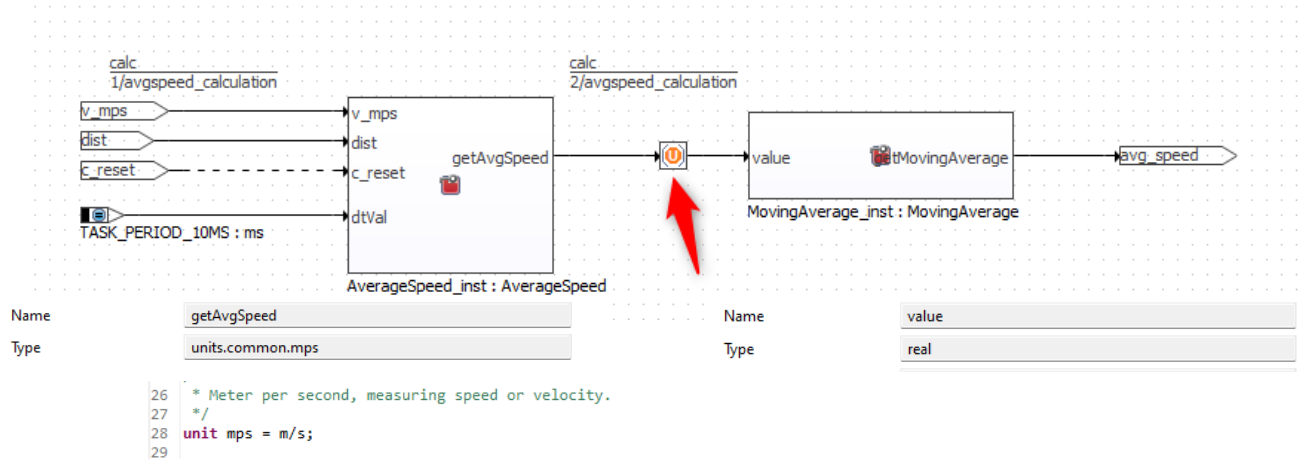
The screenshot displays the state machine editor interface. The main window shows a statechart with four states: **temperature**, **avgSpeed**, **speed**, and **distance**. Each state has an entry action and a static action. Transitions between states are triggered by the `keyPressed()` event. A transition from **temperature** to **avgSpeed** is guarded by the condition `trigger100ms && t_air < 1.0 && !frostWarning {frostWarning = true;}`. The **Class Element** properties view at the bottom shows the `frostWarning` variable, which is a `boolean` type with a default value of `false` and is set to `Private` visibility. A red circle with the number '2' is placed over the visibility options. On the right, the Outline view shows the project structure, with a red circle and the number '1' highlighting the `frostWarning : boolean` element.

Pain Point

- ☹️ Extra modeling effort for type conversion between unit less and unit type element

Benefit

- 😊 Improved user experience
- 😊 Cleaner block diagram



New features and other improvements

Pain Point

- ☹ Cannot configure for individual mapped ASCET element which RTE access type to use
- ☹ Too many manual operations to create ASCET AUTOSAR structure

Benefit

- 😊 Customizable and easy to configure element wise access
- 😊 Select ESDL Messages in mapping and create AR interfaces easily
- 😊 Generate complete AR structure as first starting point from app

The screenshot displays the Eclipse IDE interface. At the top, a code editor shows the implementation of the `MySwc` class, which is a singleton and implements the `Runnable` interface. It features several annotations for AUTOSAR: `@ArRequiredPortPrototype`, `@ArProvidedPortPrototype`, `@ArRunnable`, and `@ArTimingEvent`. The `runnable()` method is implemented with logic to manage references to `rp_sri.element1` and `pp_sri.element2`.

Below the code editor, the IDE's configuration panels are visible. The **Method** panel shows the `runnable()` method is marked as **Runnable**. The **Events** panel shows a configuration for an event named `event_10ms` with a **Kind** of `Timing` and a **Period** of `0.01` seconds.

The **Access** panel is highlighted in yellow and lists the following access types and their corresponding references:

Access	Reference
Data Read Access	rp_sri.element1
Data Receive Point by Value	rp_sri.element2
Data Receive Point by Argument	rp_sri.element2
Data Write Access	pp_sri.element1
Data Send Point	pp_sri.element2

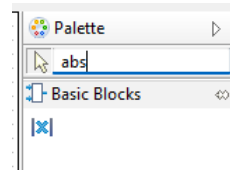
The **Sender Receiver Interfaces** panel shows a table of interfaces for the `LightAlgoSWC.ascet2autosar` project:

Access	Type	Message
R	SIG...	Light_q
R	A_Li...	LightDark_pls
R	STA...	LightState_pls

A context menu is open over the `LightState_pls` interface, showing options such as `Undo`, `Redo`, `Delete`, `Show Read Messages`, `Show Write Messages`, `Show Read/Write Messages`, `Qualified names`, `Automapping SRI Ports`, `Create new Sender Receiver Interface`, and `Add to existing Sender Receiver Interface`.

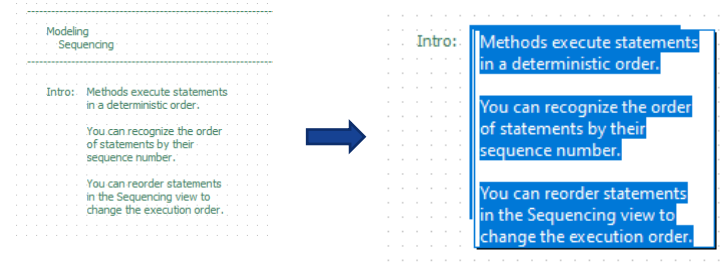
– Search in BD Editor Palette

☺ *Find block faster*



– Edit graphical comment directly in BD Editor canvas

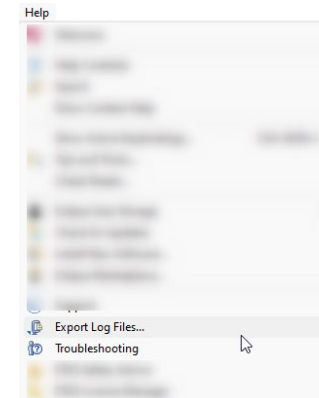
☺ *Faster operation avoid shift focus to properties view*



– Problem Report Export from Help Menu

☺ *Provide debug relevant info to etas support easier*

☺ *Direct link to troubleshooting chapter*



Thank you